

Power Level Controlling of First Amplification Stage for an Integrated RF Power Amplifier

Field of the Invention

[001] The invention relates to the field of power amplifier circuits and more specifically to the field of controlling of amplification stages forming a power amplifier in order to attain a predetermined range of output signal power.

Background of the Invention

[002] For many applications, Radio Frequency (RF) Power Amplifiers (PAs) are required to have an output signal power that is independent of PA supply voltage and PA operating temperature.

[003] Prior art PA circuits generally have a first stage that is supplied with a ramped voltage supply that is used to control an output signal of the first stage in a controllable manner. Unfortunately, a disadvantage of the old technology is that fine control for controlling of amplitude of the output signal is not easily attained. A collector emitter saturation voltage of the first stage RF transistor, or transistors, limits the first stage output signal. At saturation, the amplitude of the output signal is hard to predict with any great accuracy. As a result, this does not provide an overall PA output signal amplitude with accuracy. This poses a particular problem when the supply voltage is very low in potential and the variability of the saturation of the PA amplification stages significantly alters the power output capability. As a result, a closely controlled PA output signal level is not readily obtained. Typically, the maximum output signal power of the PA is proportional to the supply voltage or a significant efficiency penalty is suffered. Having the output signal power vary upon power supply variations is unacceptable for many applications.

[004] In cellular telephone handsets and other wireless applications, because of battery power there is provided to circuitry therein a particularly wide range of supply voltages. As a result, there is a considerable difference between the PA supply voltage when a cellular telephone handset battery is fully charged and significantly discharged.

[005] A need therefore exists to provide circuitry that during operation thereof provides a RF output signal that is approximately independent of the actual supply voltage potential. It is therefore an object of the invention to provide an input stage for an integrated PA with a more accurately controllable output signal power than is currently attainable in the state of the art.

Summary of the Invention

[006] In accordance with the invention there is provided a power amplifier circuit comprising: an input port for receiving a RF input signal; an output port for providing therefrom a RF output signal, the RF output signal being an amplified version of the RF input signal; a supply voltage input port for receiving a supply voltage; a controllable current source having an input port for receiving a control signal and an output port for providing of a variable bias current therefrom, the variable bias current based upon the control signal; a first amplification stage having a first variable gain and for receiving the RF input signal and for providing a first amplified RF signal, the first amplification stage coupled to the controllable current source for receiving the variable bias current therefrom and for having the first variable gain thereof varied in proportion to the variable bias current; a second amplification stage having a second gain and coupled to the first amplification stage for receiving the first amplified RF signal and coupled to the output port for providing the output signal thereto; and, a control circuit for generating the control signal for provision to the controllable current source, the control signal for being generated in dependence upon the supply voltage, where for the supply voltage having a first potential the variable bias current provided to the first amplification stage is smaller than for the supply voltage having a second potential that is lower than the first potential.

[007] In accordance with the invention there is provided a circuit for biasing a power amplifier circuit comprising a first amplification stage and a second amplification stage, the circuit comprising: a current source comprising: a current source input port for receiving a control signal, and an output port for providing a variable bias current in dependence upon the control signal; and, a current source control circuit comprising: a

supply voltage input port for receiving of a supply voltage, a control signal output port coupled to the current source input port for providing of the control signal to the current source, and current control circuitry for sensing a potential of the supply voltage at the supply voltage input port and for generating the control signal, where the control signal is for resulting in an increasing variable bias current with a decreasing supply voltage sensed on the supply voltage input port which results in the second amplification stage to transition from a linear mode of operation to a saturation mode of operation.

[008] In accordance with the invention there is provided a method of amplifying a RF input signal to form a RF output signal comprising the steps of: sensing of a supply voltage potential; determining whether the sensed supply voltage potential is one of higher than a first predetermined potential, in between the first predetermined potential and a second predetermined potential and below the second predetermined potential; amplifying the RF input signal with a first amplification stage having a first variable gain to form a first amplified signal, the first variable gain dependent upon the sensed supply voltage potential; amplifying the first amplified signal with a second amplification stage having a second gain to form the RF output signal; adjusting a bias current provided to the first amplification stage for varying the first variable gain in such a manner that at the first predetermined potential a lower bias current is provided to the first amplification stage than is provided to the first amplification stage at the second predetermined potential, the lower bias current for operating of the second amplification stage in a linear mode of operation and a higher bias current for operating of the second amplification stage in a saturation mode of operation.

Brief Description of the Drawings

[009] Exemplary embodiments of the invention will now be described in conjunction with the following drawings, in which:

[0010] FIG. 1a illustrates a power amplifier circuit having an input amplification stage and an output amplification stage in accordance with a first embodiment of the invention;

[0011] FIG. 1b broadly outlines operating steps of the amplifier circuit shown in FIG 1a;

[0012] FIG. 2a illustrates the control circuit, in accordance with a second embodiment of the invention, for controlling a controllable current source used for providing a bias current to the first amplification stage;

[0013] FIG. 2b illustrates the control circuit, in accordance with a third embodiment of the invention, for controlling a controllable current source used for providing a bias current to the first amplification stage using a charge pump and ramp control circuit as well as a second multiplier circuit;

[0014] FIG. 3a illustrates a relationship between supply voltage potential (V_{cc}), a sense signal (I_{sense}), output power provided from the first stage (P_{out1}), output power provided from the second amplification stage (P_{out2}), and a control signal ($I_{control}$) provided from the control circuit shown in FIGs 2a or 2b;

[0015] FIG. 3b illustrates a waveform of an enable signal applied to the enable port of the control circuit shown in FIG. 2b;

[0016] FIG. 3c illustrates a delayed turn on and a delayed turn off control signal provided from the control circuit shown in FIG. 2b;

[0017] FIG. 3d illustrates a programmable control signal that is provided to a controllable current source for controlling a gain of the first amplification stage; and,

[0018] FIG. 4 illustrates a fourth embodiment of the invention, a power amplifier circuit for operating in accordance with two different RF transmission standards.

Detailed Description of Embodiments of the Invention

[0019] FIG. 1 illustrates a power amplifier circuit 100 having a first amplification stage 101 and a second amplification stage 102 in accordance with a first embodiment of the invention. A first inter stage matching circuit 103 is disposed between the two stages, 101 and 102, for matching of impedance of connected ports therebetween. First and second

output ports, 100c and 100d, of the second amplification stage 102 provide first and second RF output signals. The first amplification stage 101 is formed from a first transistor 111 and a second transistor 112, where a base terminal of the first transistors 111 serves as a first input port 100a and a base terminal of the second transistor 112 serves as a second input port 100b. Each transistor, 111 and 112, is disposed between a controllable current source 104 and a respective reactive element 105a and 105b, where the first and second reactive elements, 105a and 105b, are connected between the collector terminals of the first and second transistors, 111 and 112, and a first supply voltage input port 100e. The controllable current source 104 is disposed between a second supply voltage input port 100f and the emitter terminals of the two transistors, 111 and 112. A control port 104a is provided on the controllable current source 104 for receiving a control current (I_{control}) from an output port 200c of the control circuit 200 (FIG. 2a, FIG. 2b), in accordance with second and third embodiments of the invention, respectively. The control circuit 200 is disposed between the first and second supply voltage input ports and is optionally provided with an enable port 200e (FIG. 2b) for enabling and disabling thereof by an external source (not shown).

[0020] The primary focus of the embodiments of the invention is the control circuit 200 (FIG. 2a) and control circuit 220 (FIG. 2b) and their use in controlling of the controllable current source 104. FIG. 2a illustrates the control circuit 200 in accordance with a second embodiment of the invention. The control circuit 200 is comprised of the following circuit blocks: a supply voltage sense circuit 201, a first multiplier circuit 202, a bandgap reference circuit 203, and a current summing circuit 204.

[0021] The supply voltage sense circuit 201 has a first input port connected to the first supply voltage input port 100e for sensing a potential of the first supply voltage (V_{cc}) applied thereto relative to a reference voltage from a reference source (not shown) provided to a second input port thereof. An output port of the supply voltage sense circuit 201 is used for providing a sense signal (I_{sense}) (302 FIG. 3a) to a first input port of a first multiplier circuit (M1) 202. Preferably M1 202 is in the form of a Gilbert cell multiplier. M1 202 additionally includes a second input port and an output port. The second input port thereof is for receiving of a first reference current $I_f(\theta)$ and the output

port thereof is for providing a first current to a first input port of the current summing circuit 204. Within the current summing circuit 204 the second reference current is summed with a portion of the first reference current to form a summed current that is provided from an output port thereof. A portion of the first reference current that forms the summed current is dependent upon the sense signal (I_{sense}) 302. In this second embodiment of the invention, the output port of the current summing circuit 204 is directly connected to the output port 200c of the control circuit.

[0022] The bandgap current reference circuit 203 is disposed in order to provide the first reference current ($I_f(\theta)$) to the second input port of the first multiplier circuit 202 and to provide a second reference current $i_f(\theta)$ to a second input port of the current summing circuit 204. First and second reference currents provided from the bandgap current reference circuit 203 are preferably temperature controlled with a controlled temperature coefficient of approximately 20% PTAT.

[0023] Broadly, the amplifier circuit illustrated in FIG 1a operates according to the following operating steps, as illustrated in FIG. 1b. In a first step, 181, the sense circuit 201 performs sensing of a supply voltage potential. A determination is then performed, in step 182, as to whether the sensed supply voltage potential is one of higher than a first predetermined potential, in between the first predetermined potential and a second predetermined potential and below the second predetermined potential. In dependence upon the determination, step 183, the RF input signal is amplified using the first amplification stage 101 having the first variable gain to form the first amplified signal, where the first variable gain is dependent upon the sensed supply voltage potential. The first amplified signal is then further amplified using the second amplification stage 102 having a second gain to form the RF output signal, in step 184. During operation of the power amplifier circuit 100 as the supply voltage potential changes, the bias current provided to the first amplification stage 101 for varying the first variable gain is adjusted in such a manner that at the first predetermined potential a lower bias current is provided to the first amplification stage 101 than is provided to the first amplification stage 101 at the second predetermined potential, the lower bias current for operating of the second amplification stage 102 in a linear mode of operation and a higher bias current for

operating of the second amplification stage 102 in a saturation mode of operation, as outlined in step 185.

[0024] FIG. 3a illustrates a supply voltage (V_{cc}) potential drop 301 from a maximum supply voltage potential 301a to a minimum supply voltage potential 301b, as well as the resulting signal power levels and current levels. The supply voltage potential drop is illustrated to be exemplary of a battery voltage drop. The supply voltage (V_{cc}) drop 301 includes two intermediate supply voltage potentials, V_{cc1} and V_{cc2} . Above V_{cc1} , a battery, for example, which provides the supply voltage to the PA 100 is fully charged and has an approximate potential of over 2.5V. Between V_{cc1} and V_{cc2} , the potential of the supply voltage drops to approximately 2V. Below V_{cc2} , the supply voltage potential drops to below approximately 2.0V.

[0025] For supply voltage potentials that are higher than the potential at V_{cc1} , the sense signal (I_{sense}) 302 provided to the first multiplier circuit 202 is at a minimal level and as a result a minimal portion of the first reference current ($I_f(\theta)$) is summed with the second reference current ($i_f(\theta)$) in the current summing circuit 204 for forming the summed current. The output power (P_{out1}) 304 provided from the first amplification stage 101 to the second amplification stage 102 is at a minimal level and as a result the second amplification stage operates in a first mode of operation, that is a linear mode of operation. Output power provide from the second amplification stage 102 is indicated in FIG. 3a as P_{out2} 303 and is substantially constant until the power supply reaches the potential V_{cc2} .

[0026] Between V_{cc1} and V_{cc2} , a controllable portion of the first reference current, ($I_f(\theta)$), is propagated through the first multiplier circuit 202 and summed with the second reference current, ($i_f(\theta)$). As the supply voltage potential 301 drops from V_{cc1} to V_{cc2} , the sense signal (I_{sense}) 302 increases in magnitude and an amount of the first reference current, ($I_f(\theta)$), that is summed with the second reference current ($i_f(\theta)$) increases. As a result, the output signal power (P_{out1}) 304 from the first amplification stage 101 increases with the increasing sense signal (I_{sense}) 302. This increase in P_{out1} 304 compensates for the decrease in the supply voltage (V_{cc}) 301 in order to maintain the

second stage output power (Pout2) 303 at a substantially constant power level. As the supply voltage declines between Vcc1 and Vcc2, the second amplification stage 102 smoothly transitions from the first mode of operation to a second mode of operation, where at Vcc2, the second amplification stage 102 only operates using the second mode of operation. The second mode of operation of the second amplification stage 102 is saturation, resulting from Pout1 304 being at a maximum. As the potential continues to drop, the second amplification stage 102 continues to operate in saturation, however, the output power (Pout2) 303 provided from the second amplification stage 102 drops in strength as a result of the supply voltage potential (Vcc) 301 decreasing past below the potential of Vcc2. Within the region of supply voltage potential (Vcc) 301 below Vcc2, the input and output amplification stages, 101 and 102, operate until the supply voltage potential (Vcc) 301 is at such a level that the power amplifier circuit 100 no longer operates.

[0027] In operation of the PA 100, the second amplification stage 102 is typically not operated at a full class 'A' compliance, but operated such that it provides a near constant power (Pout2) 303 when biased from its current source (not shown), which preferably provides a bias current thereto that is proportional to absolute temperature (PTAT). By providing the sense signal (Isense) 302 to the controllable current source 104 a corresponding bias current is provided to transistors, Q1 111 and Q2 112. This advantageously allows for a near constant output power (Pout2) 303 to be provided from the PA 100 over temperature, process and supply voltage (Vcc) variation. Over a range of input voltages for first and second input signals provided to the first and second input ports, 100a and 100b respectively, the first and second transistors Q1 111 and Q2 112 are fully switched by the input signals. As a result, the first and second output signals propagated from the first amplification stage 101 are independent of the first and second input signal levels.

[0028] FIG. 2b illustrates the control circuit 220 in accordance with the third embodiment of the invention. The control circuit 220 includes the circuitry of control circuit 200, but further comprises a second multiplier circuit 205, a charge pump and ramp control circuit 206 and an integrating capacitor 207. The second multiplier circuit

205 has a first input port, a second input port and an output port. Preferably the second multiplier circuit 205 is an analog multiplier circuit, preferably in the form of a Gilbert gain cell. The summed current provided from the output port of the current summing circuit 204 is provided to the first input port of the second multiplier circuit 205. The output port of M2 is directly connected to the output port 200c of the control circuit. An output signal from the second multiplier circuit 205 serves as the control signal (I_{control}) that is provided to the control port 104a of the controllable current source 104 used for biasing of transistors Q1 111 and Q2 112 (FIG. 1). The control signal (I_{control}) provided to the controllable current source 104 is directly proportional to the sense signal (I_{sense}) provided from the supply voltage sense circuit 201 to the first input port of M1 202. The charge pump and ramp control circuit 206 receives the enable signal via the enable port 200e from an external source (not shown) and generates a ramp signal from an output port thereof that is connected to the second input port of M2 205. A capacitance of the integrating capacitor 207 determines characteristics of the ramp signal. Control circuit 220 is optionally used in place of control circuit 200 in the PA 100 of FIG. 1.

[0029] The control circuit 220 provides a delayed turn on and a delayed turn off control signal, as shown in FIG. 3c, in response to the enable signal, shown in FIG. 3b, applied to its enable port 200e. At time t_1 , the enable signal experiences a first transition from logic LO to logic HI. This first transition results in the control signal (I_{control}) to experience a delayed ramp up from a first signal level to a second signal level, where the second signal level is achieved at a rise time of $t_1 + \Delta$. Once the enable signal experiences a second transition from logic HI to logic LO at time t_2 , the control signal experiences a delayed ramp down from the second signal level to the first signal level, having a fall time between times t_2 and $t_2 + \Delta$. The ramp time (Δ), for both the rise time and the fall time, is determined by the integrating capacitor 207. Optionally, by deliberate mismatching characteristics of transistors that form the second multiplier circuit 205, a normally linear relationship thereof is distorted so that a start of an 'on' ramp 301 and the end of an 'off' ramp 302 are more gradual.

[0030] For example, for supply voltage potentials that are higher than V_{cc1} , approximately 40mA is provided from the controllable current source 104 to the emitter

terminals of transistors Q1 111 and Q2 112. At a lower supply voltage potential, V_{cc2} , approximately 80mA of current is provided from the controllable current source 104 to the emitter terminals of transistors Q1 111 and Q2 112.

[0031] For a constant supply voltage provided to the supply voltage input ports, a small positive temperature coefficient for transistors Q1 and Q2 is preferable, such as 20% PTAT. In such a case, the output power (P_{out1}) of the first amplification stage 101 is approximately constant over temperature. This temperature coefficient of the first amplification stage 101 compensates for the performance variations of the second amplification stage 102 with temperature.

[0032] Current control of the first amplification stage is used to accurately control the output power (P_{out1}) provided from the first amplification stage 101 to the second amplification stage 102 over a wide range of output signal powers (P_{out2}). Additionally, by pre-characterizing of the second amplification stage 102, first order corrections are performable within the first amplification stage 101 for correcting variability within the second amplification stage 102 with respect to supply voltage and temperature variations. This degree of control is not possible with a voltage limited first amplification stage 101 and allows the PA 100 to operate very close to a regulatory maximum output signal power, thereby maximizing a transmitting range of the PA when used within a wireless transmitter such as those consistent with DECT or 2.4GHz DSSS.

[0033] FIG. 4 illustrates a fourth embodiment of the invention, a PA 400 for operating at two different RF transmission standards. Circuit components designated by a number that is the same in FIG. 1 include similar circuitry and perform a similar function. In addition to the circuitry of FIG. 1, FIG. 4 comprises a switching circuit 401 a second inter stage matching circuit 403 and a third amplification stage 402. First and second output signals provided from the first amplification stage 101 are received by the switching circuit 401. In dependence upon an operating standard for the PA 400, either the second amplification stage 101 or the third amplification stage are switchably coupled to the first amplification stage for receiving of the output signal from the pair of transistors Q1 111 and Q2 112. For example, the second amplification stage 102 is for operating in

compliance with the GSM standard and the third amplification stage is for operating in compliance with the CDMA standard. In dependence upon a standard at which the PA 400 is to be used, the switching circuit switchably selects the appropriate amplification stage. The second inter stage matching circuit 403 facilitates signal matching of input and output port characteristics of the third amplification stage to the first amplification stage 101. Otherwise, operation of the control circuit 200 for the fourth embodiment of the invention is similar to the operation of the control circuit for the first embodiment of the invention.

[0034] Providing an input amplification stage 101 for an integrated PA 100 with a controllable output signal power achieves control of the output signal emitted from the PA output ports 100c and 100d. Optionally, the control circuit 220 provides a programmable control signal (I_{control}) (FIG. 3d) to the controllable current source 104. Programmable control of the controllable current source 104 advantageously provides for ramping of P_{out1} in a controllable manner that generates low spurious. Further advantageously, variability of the second amplification stage 102 with respect to supply voltage and temperature fluctuations is also reduced. This improved immunity of the PA to supply voltage and temperature fluctuations is achieved when the supply voltage potential is low and the second amplification stage 102 operates in saturation. Furthermore, setting of the PA output signal power regardless of the RF input signal power is also attainable by using this programming capability. Optionally, a lookup table (LUT) is disposed within the control circuit 220 for providing of the programmable control signal.

[0035] Advantageously, the embodiments of the invention allow for designing a PA in accordance with tight specification while still allowing operation of the PA well into saturation. PA efficiency is also advantageously maintained at low supply voltage potentials.

[0036] Numerous other embodiments may be envisaged without departing from the spirit or scope of the invention.